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/Claudia Bader/ — Claudia Bader

March 2, 2011 — Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	
Hannes P. Hofmann	:	Group Art Unit: 3742
Serial No.: 10/587,691	:	Examiner: Hung D. Nguyen
Filed: 27 July 2006	:	Confirmation No.: 7045

For: METHOD OF MANUFACTURING A CIRCUIT CARRIER AND THE USE OF THE METHOD

VIA EFS
Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This brief is submitted in connection with the appeal of the above-identified application. The Notice of Appeal was filed by EFS on January 21, 2011. Accordingly, the present paper is timely filed without extension of time. The Board of Patent Appeals and Interferences is respectfully requested to reverse all of the rejections of the claims in the final Office Action mailed October 12, 2010, for the reasons set forth herein.

I. Real Party in Interest

The real party in interest in the present appeal is Atotech Deutschland GmbH, D-10507 Berlin, Erasmusstraβe 20, 10553 Berlin, Federal Republic of Germany, assignee of the present application.

II. Related Appeals and Interferences

Appellant, Appellant's undersigned representative, and/or the assignee of the present application are unaware of any other prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by, or have bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-24 are in the instant proceeding and are pending in the application. Claims 1-24 stand finally rejected and are the subject of this appeal.

IV. Status of Amendments

No amendments to the claims or the specification have been made subsequent to the final rejection contained in the Final Office Action dated October 21, 2010. An after-final Reply to Office Action was filed on November 11, 2010, but contained no amendments and did not result in any change in position of the Examiner in the Advisory Action mailed December 6, 2010.

V. Summary of the Claimed Subject Matter

Independent claim 1, the only independent claim, recites a method of manufacturing a high density circuit carrier (p. 9, lines 16-17), said method comprising the following method steps:

a) Providing a printed circuit board having circuit traces on at least one side thereof (p. 9, lines 20-28; p. 10, lines 18-29);

b) Coating the printed circuit board on the at least one side thereof with a dielectric to form a dielectric layer over the circuit traces (p. 23, line 34;

c) Structuring the dielectric layer for producing trenches and vias therein using laser ablation, the trenches not extending completely through the

dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces (p. 17, lines 9-10; p. 19, lines 1-17);

d) Depositing a primer layer onto the entire surface of the dielectric layer (p. 21, lines 1-6) or depositing the primer layer into the produced trenches and vias only (p. 20, lines 1-2 and 33-34);

e) Depositing a metal layer onto the primer layer, with the trenches and vias being completely filled with metal for forming conductor structures therein (p. 21, lines 16-18); and

f) Removing the metal layer and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step d) (p. 22, lines 12-17).

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1, 10, 12-14, 21 and 24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636).

Claims 2-11, 15 and 18-22 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Tamm et al. (US 5666722).

Claim 16 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Konrad et al. (US 2002/0129972).

Claim 17 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Yokogawa et al. (US 6740416).

Claim 23 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Frank et al. (US 5577309).

VII. Argument

A. Overview of the Claimed Invention and Prosecution History

In summary, the claims relate to a method for manufacturing a high density circuit carrier as an additional structure applied to a preexisting, conventional printed circuit board. By starting with a conventional printed circuit board as a base layer to form thereon additional signal layers having extremely fine conductor structures in accordance with the method of the invention, several benefits accrue. With the present invention, it is possible both to manufacture circuit carriers with the integration density required for a computer system board, for example, and to manufacture such circuit carriers at a high yield. These benefits accrue even if ultra-HDI conductor structures are to be produced, e.g., with lines and spaces below 50 um each, in order to allow mounting and electrical connection of complex semiconductor chip packages.

Thus, according to the invention, first a conventional printed circuit board, e.g., a multilayer board, is manufactured using well-established manufacturing techniques. This circuit board can be examined as to the absence of defects prior to forming the HDI signal layers on the outer sides thereof. Second, this circuit board will then be further processed, as described in the claims, by applying the dielectric, structuring the dielectric and forming the conductor structures in the recesses formed in the dielectric. It is not required that the conventional circuit board be provided with conductor structures of the HDI-type. Rather, the HDI-type conductor structures are formed on the outer sides of the circuit board by performing the method steps b) through f) of the claimed invention.

Thus the use of a conventionally manufactured printed circuit board as a base layer enables the inexpensive, conventional non-HDI printed circuit board to be made into a high-tech circuit carrier, provided with finest conductor structures on the outer sides thereof. This metamorphosis is performed by a relatively easy and cost-effective method while maintaining a high production yield, in accordance with the claimed invention.

The claims of the present application have been erroneously rejected in the Office Actions under 35 USC § 103(a) as being unpatentable over an ever-shifting set of prior art references. After each Reply to Office Action was filed, the next Office Action presented a wholly new combination of prior art references. The

Appellant has made every possible effort to clarify the distinctions of the claimed invention with respect to each of the newly arrayed combination of prior art references, only to be met with repeated rejections. None of the rejections has merit, in Appellant's view, including the most recent rejections.

Appellant submits that the rejections set forth in the final Office Action are based on a clearly erroneous interpretation of the combination of the primary and secondary prior art references (Clothier and Asai) that lacks support of any evidence and is clearly repudiated by the cited reference itself. All of the rejections of all the pending claims are based on this combination of Clothier and Asai, so the following arguments focus on the asserted combination of Clothier and Asai Since, without the erroneously interpreted disclosure of Clothier and attempted combination with Asai, there is no longer any basis for rejection of Appellant's claims in any combination of the asserted prior art references, the rejections should be reversed. The rejections of the claims should be reversed for at least the following detailed reasons.

B. Rejection of claims 1, 10, 12-14, 21 and 24 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) should be reversed.

Claims 1, 10, 12-14, 21 and 24 stand erroneously rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier (US 2002/0177006) in view of Asai (US 6240636). Reversal of the rejection of these claims is respectfully requested for at least the following reasons.

1. The Primary Rejection.

Regarding claim 1, the Office Action contended that Clothier discloses a process and structure as claimed, but admitted that Clothier fails to disclose providing a PCB having circuit traces on at least one side thereof, fails to disclose structuring the dielectric layer for producing vias, and fails to disclose the vias extending through the dielectric layer to the circuit traces. The Office Action contended that Asai makes up for these deficiencies, in that it discloses in Fig. 1 providing a PCB with circuit traces 3 on at least one side thereof and structuring the dielectric layer for producing vias 5 using laser ablation and the vias 5 extending through the dielectric layer to the circuit traces. Based on this, the Office Action concluded that it would have been obvious to apply Asai's process to Clothier, and

that Appellant's claimed invention therefore would have been obvious over this combination.

Appellant respectfully disagrees for several reasons.

2. The Rejections Based on Clothier Are Clearly Erroneous.

Clothier discloses, in Fig. 2A-2E, a foil 1 on which a conductive layer 2, e.g., of copper, is formed [0039]-[0040]. A dielectric layer 3 is formed on the conductive layer 2, and is shaped to form circuit features 4 [0041]. A conductive material 5 is applied over the shaped dielectric layer [0046], optionally preceded by a seed layer (not shown) [0045]. The plated conductive material 5 is then planarized with CMP to form the high density circuitry structure 10 [0047]. While this might possibly be construed to show forming trenches and filling them, it is only part of what Clothier discloses, and the process of Clothier does not and cannot stop at this point. Following these initial steps, as shown in Figs. 2F-2O, two of the structures 10 are sandwiched together with a dielectric layer 6 between them to form a two-layer structure 22. Then, as shown in Figs. 2M-2O, vias are formed all the way through to the circuit traces.

Alternatively, the structure 10 can be employed as a single layer, with the dielectric layer 6 being applied to the flush planar surface 8 of a single layer. Since the following description does not otherwise differentiate between the single layer and double layer structure, the following steps, including the vias being formed all the way through to the circuit traces, must be the same.

Appellant respectfully submits that, when comparing the present invention with the methods disclosed by Clothier et al. and Asai et al., there is remarkable, distinguishing difference to be considered, and that the Office action failed to consider or even recognize this difference. This difference shows that the references fail to disclose or suggest all of the features of claim 1 and of the claims dependent thereon of the present application. Accordingly, there is no basis for a *prima facie* case of obviousness, and the rejections of Appellant's claims should be reversed.

The Office action alleges that it would have been obvious to one of ordinary skill in the art to utilize in Clothier et al., providing a PCB having circuit traces on at

least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces, as taught by Asai.

In order to come to this conclusion, Appellant submits that a person skilled in the art would have to replace some item used in the Clothier method by the PCB of Asai, and then structure the dielectric layer of Clothier for producing the vias extending through to the circuit traces.

Such item to be replaced could only be the carrier 1 and conductive layer 2 of Clothier onto which the dielectric 3 is applied.

The Office action failed to note, however, the specific function of the carrier foil 1 and conductive layer 2 of Clothier, to which then the dielectric material 3 is applied, which in turn is structured and finally filled with conductive material 5.

If a person skilled in the art would – as the Office action contends – provide the PCB having circuit traces on at least one side thereof of Asai et al., and structure the dielectric layer for producing vias such that the vias extend through the dielectric layer to the circuit traces, as Asai teach, this person would, to combine the two references, require in the other (Clothier) reference a process which comprises starting with a base material which could be replaced by the PCB of Asai. In order to be replaced by the PCB of Asai et al., the respective base material of this other reference would have to become a functional entity of the final circuit carrier to be produced since Asai teach to have the PCB (wiring pattern 3) being a functional entity of the final circuit carrier. And so does the present invention.

This could not be done.

But in fact, Clothier starts with a base material (carrier foil 1 and conductive layer 2) which would not be replaced by the PCB of Asai because this base material is removed prior to finishing the final circuitry in the method of Clothier. The base material of Clothier simply helps manufacturing the circuitry structure (temporarily impart the elements thereof mechanical stability) and therefore will not be a part of the final structure: Clothier starts with a carrier foil made of copper which carries a conductive layer, made of chromium. This ensemble is removed in the method step from Fig. 2F to Fig. 2G and is no longer used in the subsequently produced circuitry structure of Clothier. By contrast, the PCB of Asai will form an integral part of the final printed circuit board. Thus, the teachings of these references are not compatible with one another, and would not have rendered obvious the invention.

Thus, in order to combine these references, such a fundamental change would be necessary in Clothier that it would completely alter the basic function of the teachings of the reference, and such extreme modification, to the point of destroying the function of the inventions disclosed in the references, is not proper for any obviousness analysis. Such a major modification would not have been obvious to a person of ordinary skill in the art, and thus the contended result of this modification would not have been obvious, either.

Therefore, for this reason, the two references, Clothier and Asai, do not suggest the combination of the method as claimed. Since all the rejections are based on this clearly erroneous combination, none of the rejections state a proper *prima facie* case of obviousness and should be reversed.

3. The Examiner Failed to Rebut Appellant's Facts and Arguments.

The Examiner responded to Appellant's arguments by first, basically reiterating the rejection, rationalizing that "since Clothier discloses all the limitations in the claim except the printed circuit board having circuit traces on at least one side thereof and structuring vias. However, Asai discloses the printed circuit board having a circuit traces on at least one side thereof and structuring the vias. The extra step provided by Clothier is irrelevant." This "argument" fails to rebut the points raised by Appellant regarding the facts showing that Clothier and Asai are incompatible, that if the printed circuit board of Asai was used in Clothier as alleged by the Examiner, it would be removed in Clothier's later steps.

Second, the Examiner responded to Appellant's argument that Clothier's base material is removed prior to finishing the final circuit by rationalizing that this step can be omitted, based on a clearly erroneous misreading of the disclosure of Clothier. The Examiner contended that removal of the base material is optional based on paragraph 49 of Clothier, which discloses "Next, the carrier foils 1 *can be* removed such as by etching in a suitable etchant." (Emphasis added.) Thus, the Examiner interprets the "can be" in this sentence to mean that the removal of the carrier foils 1 is optional. This is an incorrect reading of this disclosure.

The Examiner rejections are clearly erroneous and not supported by substantial evidence, and the Examiner's arguments fail to rebut Appellant's facts and arguments, for at least the following reasons.

First, the Examiner's interpretation of the "can be" in [0049] is clearly incorrect and is not in accordance with the English language. Appellant respectfully submits that this is interpretation is clearly erroneous and without support of any evidence, much less substantial evidence. The "can be" in [0049] does not mean the step is optional; rather, it means that removal of the carrier foil by etching is *one way* that it can be removed, which suggests that other methods might be possible. Paragraph [0049] reads as follows:

> [0049] Next, the carrier foil 1 *can be* removed such as by etching in a suitable etchant (see FIG. 2g). The layer 2 such as the chromium acts as an etch mask to protect the underlying conductive material 5 during the removal of carrier foil 1. The layer 2 is a different material than foil 1 and conductive material 5. (Emphasis added.)

Quite clearly, this disclosure means that when the carrier foil 1 is removed, the removal *can be* carried out by a method such as etching in a suitable etchant, or by some other suitable method *This does not mean that the removal of the carrier foil 1 is optional.* Any such interpretation is without support of any evidence and is clearly erroneous. Fig. 2g, specifically referred to in [0049] of Clothier, shows that the carrier foil 1 has been removed. There is nothing anywhere in Clothier to suggest an embodiment in which the carrier foil 1 is not removed. There is no disclosure, no suggestion, nothing whatsoever in Clothier to suggest that removal of the carrier foil 1 might be optional. There is no illustration of such an embodiment. It is simply not there, and it is wrong for the Examiner to contend that such is possibly within the scope of the disclosure of Clothier. It is <u>not</u>.

In fact, paragraph [0048] describes the application of a layer 6 of a dielectric material such as a pre-preg, and states that the layer 6 also provides mechanical robustness needed for the following processing. Such following processing is described in the very next paragraph, i.e., [0049], which describes the removal of the carrier foil 1. Without the carrier foil 1, in the absence of the layer 6, the layers remaining would have little if any robustness.

Further, as shown in Fig. 2h and described in paragraph [0050] of Clothier, following removal of layer 1 and addition of layer 6, even the layer 2 is removed. It would be impossible to remove the layer 2 if the layer 1 were still present. This is further evidence that Clothier fails to disclose or suggest any possibility that layer 1 might not be removed.

Furthermore, the same "*can be*" language in setting forth optional ways to carry out required steps is used throughout Clothier. These uses do not even remotely suggest that any of the steps described might be optional. See, e.g., [0040], "An example of a suitable electrically conductive layer 2 is chromium which *can be* deposited by sputtering or evaporation." See, e.g., [0042], "For example, any of the known techniques for laser ablating *can be* employed." See, e.g., [0045], "The top surface and circuit features *can* then *be* seeded (not shown) by depositing a relatively thin seed layer of a conductive metal." See, e.g., [0046], "The conductive film *can be* deposited by electroless plating, electroplating, sputter coating or evaporation techniques that are well known in the art." (Emphasis added in all instances.) None of these uses of "can be" in any way suggest that the step is optional. Rather, all imply that what follows are suggested examples, and that other ways are possible. The mere fact that the drafter of the Clothier specification used the terminology "can be" in enumerating ways to carry out required steps does not and cannot possibly convert those required steps into optional steps.

For the foregoing reasons, Appellant respectfully submits that the Examiner's arguments fail to rebut Appellant's arguments, that the interpretation asserted by the Examiner is clearly wrong and without support of any evidence.

Accordingly, the presently claimed invention cannot have been obvious over Clothier in view of Asai.

Second, in asserting the combination of Clothier and Asai, the Examiner has failed to consider that Asai requires the process to begin with a copper foil 1 on the outer surface of the insulating resin layer 2 (which appears to be considered by the Examiner to correspond to Appellant's dielectric layer), which are together bonded to the inner wiring pattern 3 and the inner resin layer 4 (col. 2, lines 58-65). In contrast, the present invention starts with a printed circuit board and simply applies a dielectric – without further outer copper layer – on this printed circuit board. Asai forms the via holes 5 through the foil 1 and the insulating layer 2 (col. 4, lines 59-63). Following this, Asai forms the outer copper layer 6 on the copper foil 1 and the insulating layer 2 by electroless plating (col. 5, lines 1-15). Asai requires this outer copper layer to form circuitry strongly adhering to the outer layer of the package to manufacture a multi-layer board (col. 5, lines 16-21).

Therefore, since the outer copper layer 1 has strong bond strength to the outer layer of copper foil, the adhesion strength between the insulating resin layer 2 and the outer copper layer 6 is higher than the case where the outer copper layer 6 is plated directly onto the resin layer 2.

In contrast, the problem of adherence of the copper circuit traces to the dielectric is solved in the present invention by embedding the circuit traces into the dielectric itself. Adherence is a problem in the method of Asai, because according to Asai the circuit traces are formed on top of the resin layer.

Thus, because very different structures are involved, the disclosures of Asai and Clothier and not combinable as asserted by the Examiner, and any resulting combination would be quite different than Appellant's claimed invention.

For this additional reason, Appellant respectfully submits that the asserted combination of Clothier and Asai would not have rendered obvious the presently claimed invention.

Third, comparison of the teachings of Clothier and Asai clearly shows that the process of Clothier would be used to form the initial structure shown in Fig. 1 of Asai, and that combining Clothier with Asai would yield nothing more than Asai's own invention, and would not yield or even lead the person of ordinary skill to Appellant's claimed invention. The trenches formed by Clothier (which allegedly meet the limitations of Appellant's claims of forming trenches not extending completely through the dielectric layer to circuit traces) *are what is used to form the circuit traces!* One cannot do both. One cannot both form trenches into which circuit traces subsequently are to be formed and, at the same time, form the trenches to not reach the not-yet-formed circuit traces. It is illogical to contend this.

Thus, neither of Clothier nor Asai teaches forming trenches that do not reach circuit traces. In Clothier, there are no circuit traces, as admitted by the Office Action. In Asai, there are no trenches that do no reach the circuit traces. Combination of Clothier and Asai does not provide the missing elements, at least not without the aid of impermissible hindsight. There is nothing in the description of the formation of circuit traces in Clothier that would suggest modification of Asai's circuit boards to form trenches as well as the vias described by Asai. Clothier's "trenches" are formed before there are any circuit traces – in fact, Clothier's "trenches" are the very location into which the not-yet-formed circuit traces will be formed when they

are subsequently formed. In Asai, the circuit traces are already formed, but there is nothing even remotely analogous to the step in Clothier of forming trenches except, as noted, in the process of forming the initial structure in Fig. 1 of Asai.

For this reason, the Office Action fails to state a proper *prima facie* case of obviousness, since the contended combination fails to show all the limitations of the claims. The best that one could get from the combined disclosures of Clothier and Asai is that Clothier teaches how to form the initial structure shown in the upper left of Fig. 1 of Asai. In other words, the disclosure of Clothier is relevant to an entirely different point in the formation of the structure of Asai, and there is nothing in either reference that discloses or suggests the claimed combination of steps.

Accordingly, the presently claimed invention cannot have been obvious over Clothier in view of Asai.

Fourth, the present invention requires that a printed circuit board is used in method step (a) and that circuitry is formed thereon in further method steps (b) through (f). This not only requires that the printed circuit board is not removed from the circuitry being formed thereon but also provides a function that a carrier foil and conductive layer do not have: The printed circuit board of the present invention provides electrical functionality in that it has an electrical wiring therein which for example electrically connects individual circuit features formed in the circuitry which is formed on the printed circuit board.

In Clothier, the carrier foil 1 typically is a copper foil (Clothier, [0039]) and the conductive layer 2 may be chromium for example (Clothier, [0040]). Thus, the carrier foil 1 and the conductive layer 2 are not able 'to selectively connect individual circuit features' as a wiring does. This is clearly in contrast to what is desired according to the present invention and why a printed circuit board is used for this purpose, namely, forming individual electrical connections between individual electrical features of the circuitry. Namely, one main aspect of the present invention is to manufacture a high density circuit carrier which has a conventionally produced printed circuit board as an inner core and which has on the outer sides thereof a high density (i.e., very fine pitch) circuitry. This construction makes easy manufacture possible, because the majority of circuitries of the circuit carrier of the invention may be produced in the conventional printed circuit board thus allowing high manufacturing yield and because fine pitch is additionally formed on the outer sides

to match semiconductor mounting thereon. Therefore, in order to have the high density circuit carrier being produced, it is mandatory for the present invention to provide a printed circuit board in method step (a) instead of a metal layer as Clothier does.

In fact, contrary to the present invention, the mere function of the carrier foil 1 of Clothier is to mechanically support the circuitry subsequently formed thereon in method steps (b) through (f). But Clothier's carrier foil 1 has no electrical function of the final circuit board being formed. Therefore, it will at least be desirable to remove the carrier foil prior to using the circuitry formed thereon because this carrier foil has no electrical function and furthermore would interfere with the circuitry formed thereon (no vias may be formed to the carrier foil since this would create shorts). And furthermore, to achieve the high density circuit carrier of the present invention would require that a printed circuit board be used instead of the carrier foil in order to provide the required wiring in the core of the finally produced board.

Therefore, according to the Examiner's argument, a printed circuit board would have to be used instead of the carrier foil in Clothier. But Clothier simply uses the carrier foil to mechanically support the circuitry formed thereon. Substitution of the carrier foil by a printed circuit board would be strange to a person skilled in the art and would therefore be non-obvious because such substitution would make no sense: A carrier foil is much less expensive and can easily be removed (by etching for example), whereas a printed circuit board might only be removed by peeling same off the circuitry, thereby giving rise to the problem that peeling mechanically would affect the sensitive circuitry adversely. Therefore, substitution of a printed circuit board the carrier foil 1 in the process of Clothier would not have been obvious.

Fifth, Appellant respectfully submits that the Office Actions have proven too much. Since Clothier clearly intends only to form vias that extend all the way through, it makes no sense to selectively stop the process of Clothier at an incomplete, initial point, and then somehow combine this with the teachings of Asai. This modification is not something the skilled person would do; rather Appellant respectfully submits it is only something that would be done in an exercise of improper hindsight.

Asai does more than simply start with a PCB with circuit traces on it, apply a dielectric and then structure the dielectric for producing vias. Rather, Asai starts with

a PCB having circuit traces 3, a dielectric layer 2, a copper foil layer 1 on the dielectric 2 and a supporting member 10 on the copper foil layer 1. Asai removes the supporting member, cuts through both the copper foil layer 1 and the dielectric 2 to reach the circuit traces 3, and then fills this. There is nothing in Asai to suggest that trenches not reaching the circuit traces might be added or used with the Asai teachings.

Thus, there is nothing whatsoever in either of Clothier or Asai to suggest the claimed process of forming both trenches and vias, in which the trenches do not extend to the circuit traces while at the same time the vias do extend to the circuit traces, as claimed. While there may arguably be a point in Clothier at which there are trenches not extending to the circuit traces, there is nothing to suggest stopping at this point in some cases while proceeding to form vias that do connect to the circuit traces in other cases. Similarly, in Asai, there is nothing to suggest that, rather than forming vias that extend to the circuit traces, one should stop in some cases and form only trenches in other cases.

For the foregoing reasons, Appellant respectfully submits that the presently claimed invention of claim 1 and of the claims dependent thereon, and particularly claims 10, 12-14, 21 and 24, would not have been obvious over Clothier in view of Asai. Appellant respectfully submits that the references fail to disclose or suggest all of the features of claim 1 and of the claims dependent thereon of the present application. Accordingly, there is no basis for a *prima facie* case of obviousness, and the rejections of Appellant's claims should be withdrawn.

C. Rejection of claims 2-11, 15 and 18-22 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Tamm et al. (US 5666722). should be reversed.

Claims 2-11, 15 and 18-22 stand erroneously rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier in view of Asai, and further in view of Tamm (US 5666722).

Claim 2 specifies that the trenches and vias are produced in one single process operation in step c). This is clearly incompatible with the combination of Clothier and Asai for the same reasons as set forth above, and Tamm fails to remedy the shortcomings of the primary and secondary references.

Claims 3-8, 18, 20 and 22 relate to use of a direct-write technique of producing the trenches and vias in step c). This is clearly incompatible with the combination of Clothier and Asai for the same reasons as set forth above, and Tamm fails to remedy the shortcomings of the primary and secondary references.

Claim 9 specifies that the trenches and vias are connected to each other in a landless design. This ensures a significant increase in conductor packaging density as well as broadening the overall process-operating window considerably, and is not compatible with the asserted combination of Clothier and Asai, and Tamm fails to remedy the shortcomings of the primary and secondary references.

Claims 10, 11 and 19 relate the another dielectric layer being deposited and steps c) through f) being repeated, and a terminating layer can be applied (claims 11 and 19). These features provide for a buildup of additional layers of circuitry and/or protection of the outer layer, and is not compatible with the asserted combination of Clothier and Asai., and Tamm fails to remedy the shortcomings of the primary and secondary references

Claim 15 specifies that in step c), when producing trenches, the trenches also comprise vias. In the thus-formed substrate, a combined trench and via is thus formed, i.e., simultaneously (see p. 15, lines 8-13 of Appellant's specification). The Office Action refers to Figs. 2b and 2c of Tamm in support of the rejection. However, Tamm discloses sequential formation of a structure that arguably contains a combined trench and via, in the description of these figures, from col. 4, line 66 to col. 5, line 4. Furthermore, the method of Tamm is not compatible with Clothier or Asai. Accordingly, Appellant submits that claim 15 would not have been obvious over the asserted combination of Clothier, Asai and Tamm.

Claim 21 specifies that the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on both sides. This is clearly incompatible with the combination of Clothier and Asai for the same reasons as set forth above, and Tamm fails to remedy the shortcomings of the primary and secondary references.

For the foregoing reasons, in addition to the reasons set forth in Section B above, Appellant respectfully submits that claims 2-11, 15 and 18-22 would not have been obvious over Clothier in view of Asai and further in view of Tamm. Accordingly, Appellant requests that the rejections of these claims be reversed.

D. Rejection of claim 16 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) and further in view of Konrad et al. (US 2002/0129972) should be reversed.

Claim 16 stands erroneously rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier in view of Asai, and further in view of Konrad (US 2002/0129972).

Claim 16 specifies that functional layers are deposited onto the metal layer for electrically contacting electric components. If the asserted combination of Clothier and Asai is made, it does not appear possible to connect the electric components as claimed, and Konrad fails to remedy the shortcomings of the primary and secondary references. Therefore, claim 16 would not have been obvious over the asserted combination for this additional reason.

E. Rejection of claim 17 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Yokogawa et al. (US 6740416) should be reversed.

Claim 17 stands erroneously rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier in view of Asai, and further in view of Yokogawa (US 6740416).

Claim 17 recites that the circuit carrier is manufactured in a horizontal line. If the asserted combination of Clothier and Asai is made, it does not appear possible to connect the electric components as claimed, and Yokogawa fails to remedy the shortcomings of the primary and secondary references. Therefore, claim 17 would not have been obvious over the asserted combination for this additional reason.

F. Rejection of claim 23 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636), and further in view of Frank et al. (US 5577309) should be reversed.

Claim 23 stands erroneously rejected under 35 U.S.C. § 103(a) as unpatentable over Clothier in view of Asai, and further in view of Frank (US 5577309).

Claim 23 specifies that the trenches and vias have a V-shape cross-section. This facilitates the electrolytic deposition of metal in the trenches and vias since the depth of the notches is small with respect to the width of their opening. Frank fails to remedy the shortcomings of the primary references, so addition of this reference would not have rendered obvious claim 23, despite that the shape of the vias may be similar.

G. Conclusion

For at least the foregoing reasons, Appellant submits that the claims of the present invention would not have been obvious over the various combinations of prior art references, and particularly over Clothier in view of Asai. Accordingly, Appellant respectfully requests reversal of all rejections contained in the Office Actions.

VIII. Claims Appendix

An appendix containing a copy of the claims involved in this appeal is attached to this brief.

IX. Evidence Appendix

An evidence appendix is attached, but identifies no items of evidence.

X. Related Proceedings Appendix

A related proceedings appendix is attached, but identifies no decisions.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of manufacturing a high density circuit carrier, said method comprising the following method steps:

a) Providing a printed circuit board having circuit traces on at least one side thereof;

b) Coating the printed circuit board on the at least one side thereof with a dielectric to form a dielectric layer over the circuit traces;

c) Structuring the dielectric layer for producing trenches and vias therein using laser ablation, the trenches not extending completely through the dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces;

d) Depositing a primer layer onto the entire surface of the dielectric layer or depositing the primer layer into the produced trenches and vias only;

e) Depositing a metal layer onto the primer layer, with the trenches and vias being completely filled with metal for forming conductor structures therein; and

f) Removing the metal layer and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step d).

2. The method according to claim 1, characterized in that the trenches and vias are produced in one single process operation in method step c).

3. The method according to claim 1, characterized in that the trenches and vias are produced using a direct-write technique in method step c).

4. The method according to claim 3, characterized in that the direct-write technique comprises scanning a laser beam across the dielectric layer at those surface regions of the dielectric layer in which the trenches and vias are to be produced.

5. The method according to claim 3, characterized in that the direct-write technique further comprises adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced.

6. The method according to claim 3, characterized in that the direct-write technique further comprises pulsing the laser beam.

7. The method according to claim 6, characterized in that the direct-write technique further comprises adjusting the energy amount of the laser beam irradiated to a surface area of the dielectric layer to depend on the depth of the trenches and vias to be produced by setting the number of laser pulses being irradiated to said surface area.

8. The method according to claim 6, characterized in that the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric layer.

9. The method according to claim 1, characterized in that the trenches and vias are connected to each other in a landless design.

10. The method according to claim 1, characterized in that the following further method steps are performed once or several times after method step f): g) Depositing another dielectric layer onto the dielectric layer being provided with trenches and vias; and h) Repeating the steps c) through f).

11. The method according to claim 10, characterized in that a terminating layer is deposited after any one of method steps f) or h).

12. The method according to claim 1, characterized in that the primer layer is deposited by performing a treatment with metal activators or with monomer solutions for forming conductive polymer layers or with carbon suspensions or by sputtering or performing by a direct deposition method.

13. The method according to claim 1, characterized in that the metal layer is formed by electroless and/or by electrolytic plating.

14. The method according to claim 1, characterized in that the metal layer and the primer layer are removed by polishing and/or by a chemical back-etching technique and/or an electrochemical back-etching technique and/or by electropolishing.

15. The method according to claim 1, characterized in that producing trenches and vias in the dielectric layer in method step c) comprises producing trenches, said trenches also comprising vias.

16. The method according to claim 1, characterized in that functional layers are deposited onto the metal layer for electrically contacting electric components.

17. The method of claim 1 wherein the circuit carrier is manufactured in a horizontal line.

18. The method according to claim 4, characterized in that the direct-write technique further comprises adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced.

19. The method according to claim 1, characterized in that a terminating layer is deposited after method step f).

20. The method according to claim 1, characterized in that the trenches and vias are produced using a direct-write technique in one single process operation in method step c).

21. The method according to claim 1, characterized in that the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side.

22. The method according to claim 7, characterized in that the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric.

23. The method according to claim 1 characterized in that the trenches and vias have a V-shape cross-section.

24. The method according to claim 1 characterized in that in method step c) the laser ablation comprises contacting the dielectric layer with a reactive gas during the laser ablation.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.